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In The Claims:

Claims 1-12 (canceled)

Claim 13 (currently amended) A trench capacitor, comprising:

a substrate having a trench;

a conducting layer filling said trench;

a first capacitor dielectric layer between a surface of said trench and said conducting layer, wherein the first capacitor dielectric layer continuously extends from inside the trench to an upper surface of the substrate;

a protruding electrode on said substrate around said trench and covering a junction of said trench and said substrate, said protruding electrode having an upper surface and a sidewall;

a second capacitor dielectric layer between said protruding electrode and said substrate, said substrate around said first and second capacitor dielectric layers being a bottom electrode; and

a conducting structure electrically connecting said protruding electrode and said conducting layer, wherein said conducting layer, said protruding electrode, and said conducting structure serve as an upper electrode, and wherein said conducting structure electrically connects said protruding electrode by contacting the upper surface of said protruding electrode.

Claim 14 (original) The trench capacitor of claim 13, wherein said protruding electrode extends to cover said conducting layer.

Claim 15 (original) The trench capacitor of claim 13, wherein said first and second capacitor dielectric layers are at least one of an oxide layer, a SiO2/Si3N4/SiO2 (ONO) stacked layer, and a Si3N4/SiO2 (NO) stacked layer.

Claim 16 (original) The trench capacitor of claim 13, wherein said conducting layer and said protruding electrode include doped polysilicon.

Claim 17 (original) The trench capacitor of claim 13, wherein said conducting structure is copper (Cu) or tungsten (W).

Claim 18-24 (canceled)

Claim 25 (currently amended) A dynamic random access memory cell, comprising:

a substrate having a trench;

a conducting layer filling said trench;

a first capacitor dielectric layer between the surface of said trench and said conducting layer, wherein the first capacitor dielectric layer continuously extends from inside the trench to an upper surface of the substrate;

a protruding electrode on said substrate around said trench and covering a junction of said trench and said substrate, said protruding electrode having an upper surface and a sidewall;

a second capacitor dielectric layer between said protruding electrode and said substrate, said substrate around said first and second capacitor dielectric layers being a bottom electrode;

a gate electrode on said substrate beside said protruding electrode;

a plurality of drain/source regions in said substrate beside two sides of said gate electrode;

a gate dielectric layer between said gate electrode and said substrate; and

a conducting structure electrically connecting said protruding electrode and said conducting layer, and said conducting layer, said protruding electrode, and said conducting structure being an upper electrode, wherein said conducting structure electrically connects said protruding electrode by contacting the upper surface of said protruding electrode.

Claim 26 (original) The dynamic random access memory cell of claim 25, wherein said protruding electrode extends to cover said conducting layer.

Claim 27 (original) The dynamic random access memory cell of claim 25, wherein said first and second capacitor dielectric layers is at least one of an oxide layer, a SiO2/Si3N4/SiO2 (ONO) stacked layer and a Si3N4/SiO2 (NO) stacked layer.

Claim 28 (original) The dynamic random access memory cell of claim 25, wherein said conducting layer and said protruding electrode include doped polysilicon.

Claim 29 (original) The dynamic random access memory cell of claim 25, wherein said conducting structure is copper (Cu) -or tungsten (W).

Claim 30 (original) The dynamic random access memory cell of claim 25 further comprising a plurality of spacers on sidewalls of said conducting layer and said gate electrode.

Claim 31 (original) The dynamic random access memory cell of claim 30 further comprising a self-aligned silicide layer on surfaces of said conducting layer and said gate electrode.

Claim 32 (original) The dynamic random access memory cell of claim 25, wherein a material of said first and second capacitor dielectric layers is the same as a material of said gate dielectric layer.

Claim 33 (original) The dynamic random access memory cell of claim 25, wherein a material of said first and second capacitor dielectric layers is different from a material of said gate dielectric layer.

Claim 34 (previously presented) The trench capacitor of claim 13, wherein said conducting structure is separated from the sidewall of said protruding electrode by an insulating spacer.

Claim 35 (Cancelled)

Claim 36 (previously presented) The dynamic random access memory cell of claim 25, wherein said conducting structure is separated from the sidewall of said protruding electrode by an insulating spacer.

Claim 37 (new) A dynamic random access memory cell comprising:

a substrate having a trench;

a conducting layer filling said trench and extending to said substrate around said trench, wherein a top surface of the conducting layer is aligned with an upper surface of the substrate;

a capacitor dielectric layer continuously extending from inside the trench to the upper surface of the substrate between a surface of said trench and said conducting layer, and between said conducting layer and said substrate, said conducting layer being an upper electrode, and said substrate around said capacitor dielectric layer being a bottom electrode;

a gate electrode on said substrate beside said conducting layer;

a plurality of drain/source regions in said substrate beside two sides of said gate electrode; and

a gate dielectric layer between said gate electrode and said substrate.

Claim 38 (new) The dynamic random access memory cell of claim 37, wherein said first and second capacitor dielectric layers is at least one of an oxide layer, a SiO2/Si3N4/SiO2 (ONO) stacked layer, and a Si3N4/SiO2 (NO) stacked layer.

Claim 39 (new) The dynamic random access memory cell of claim 37, wherein a material of said capacitor dielectric is the same as a material of said gate dielectric layer.

Claim 40 (new) The dynamic random access memory cell of claim 37, wherein a material of said capacitor dielectric is different from a material of said gate dielectric layer.

Claim 41 (new) The dynamic random access memory cell of claim 37, wherein said conducting layer and said gate electrode include doped polysilicon.

Claim 42 (new) The dynamic random access memory cell of claim 37 further comprising a plurality of spacers on sidewalls of said conducting layer and said gate electrode.

Claim 43 (new) The dynamic random access memory cell of claim 23 further comprising a self-aligned silicide layer on surfaces of said conducting layer and said gate electrode.